Lecture 8
MSP430 peripherals – III

Atul Lele

Ramakrishna Reddy

14th September 2011

Outline

- Summary from previous session/s.
- Agenda for this session.
  - MSP430 peripherals – III
    - DMA
    - LCD
- Wrap-Up.
- Q&A

Summary from previous session/s

Summary from previous session/s

- Low Power Embedded Systems and Applications
- MSP430 Architecture, Instruction Set, Clock System, Memory map
- MSP430 Family
- Programming MSP430 using CCS
- Low Power Modes and Interrupts
- MSP430 Peripherals I
- MSP430 Peripherals II

Agenda for this session

Agenda for this session

- MSP430 peripherals – III
  - DMA
  - LCD
  - RTC

DMA (1/5)

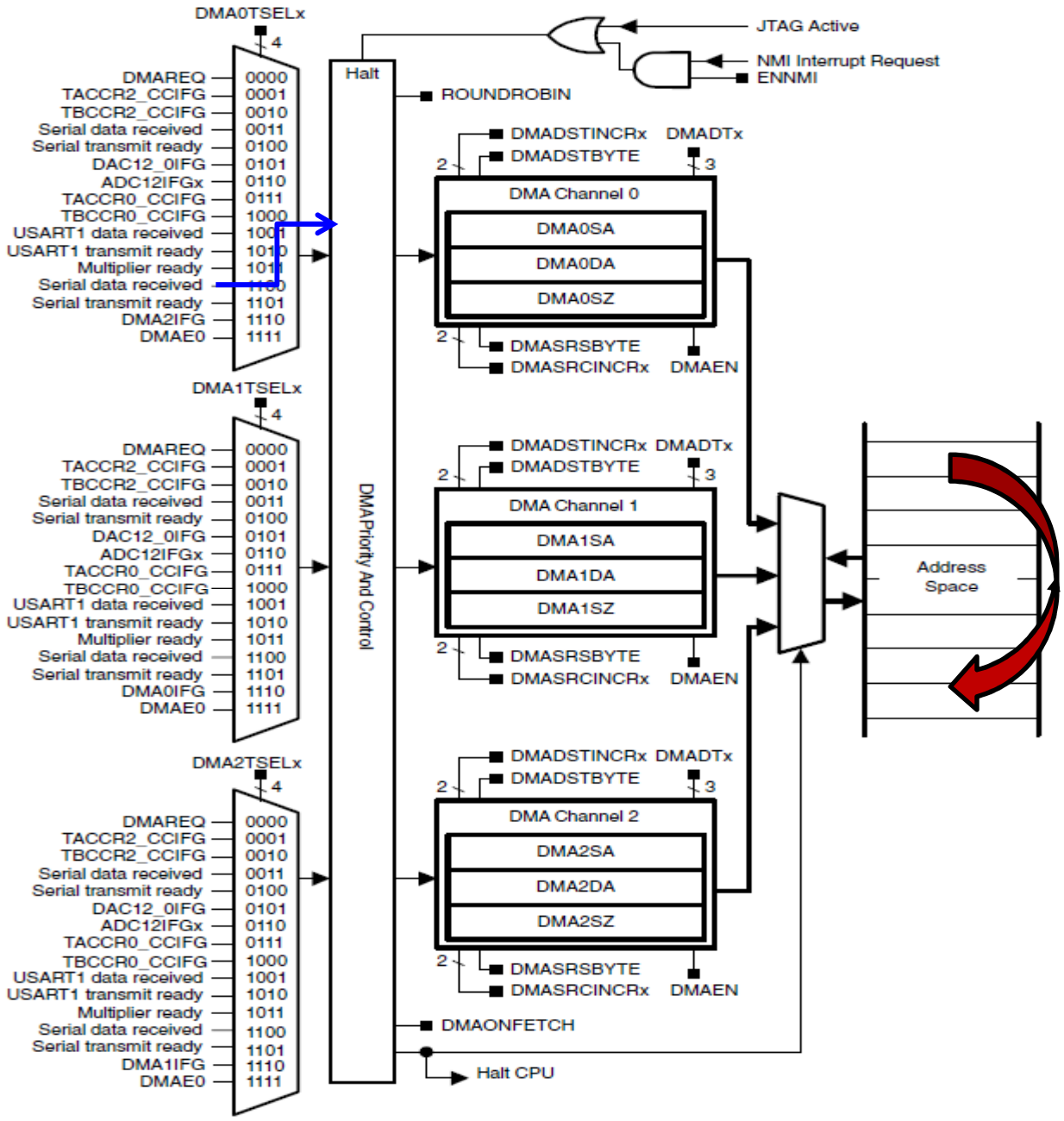
- The **D**irect **M**emory **A**ccess (DMA) controller transfers data from one address to another, without CPU intervention, across the entire address range.
  - E.g. The DMA controller can move data from the ADC12 conversion memory to RAM.
- Devices that contain a DMA controller may have one, two, or three DMA channels available.
- Using the DMA controller can increase the throughput of peripheral modules.
- It can also reduce system power consumption by allowing the CPU to remain in a low-power mode without having to awaken to move data to or from a peripheral.

DMA (2/5)

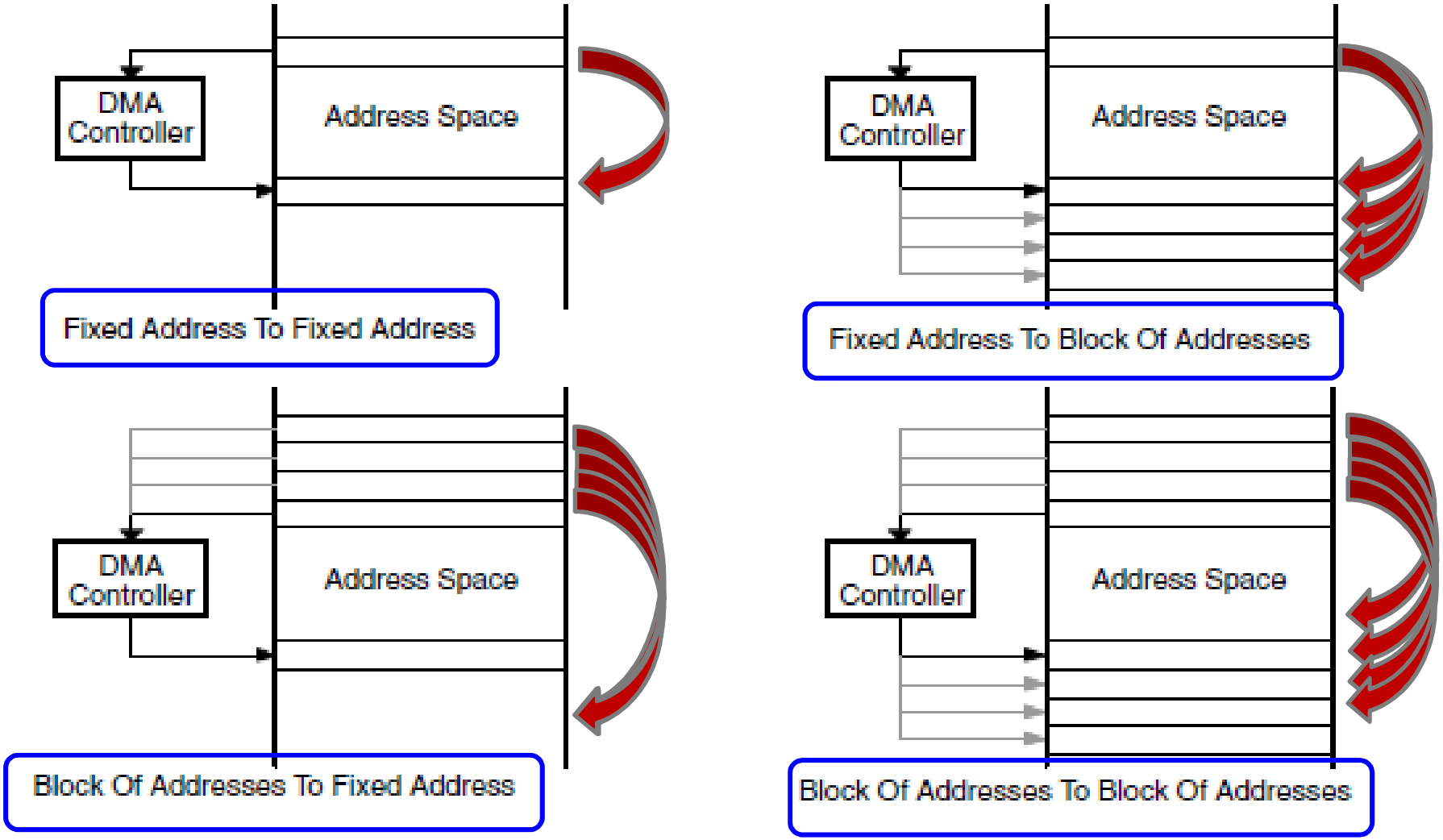
- DMA Features
  - Up to three independent transfer channels
  - Configurable DMA channel priorities
  - Requires only two MCLK clock cycles per transfer
  - Byte or word and mixed byte/word transfer capability
  - Block sizes up to 65535 bytes or words
  - Configurable transfer trigger selections
  - Selectable edge or level-triggered transfer
  - Four addressing modes
  - Single, block, or burst-block transfer modes

DMA (3/5)

1. Initial State/Reset
2. DMA Configuration
   - Upto 3 channels
3. Idle
4. Wait for Trigger
5. Hold CPU, & Transfer



DMA (4/5) → Addressing Modes



DMA (5/5) – Transfer Modes

	Type	Description
1	Single Transfer	Each transfer requires a trigger. DMAEN is automatically cleared when DMAxSZ transfers have been made.
2	Block Transfer	A complete block is transferred with one trigger. DMAEN is automatically cleared at the end of the block transfer.
3	Burst Block Transfer	CPU activity is interleaved with a block transfer. DMAEN is automatically cleared at the end of the burst-block transfer.
4	Repeated Single Transfer	Each transfer requires a trigger. DMAEN remains enabled
5	Repeated Block Transfer	A complete block is transferred with one trigger. DMAEN remains enabled
6	Repeated Burst Block Transfer	CPU activity is interleaved with a block transfer. DMAEN remains enabled.

LCD_A (1/10)

- The LCD_A controller directly drives LCD displays by creating the ac segment and common voltage signals automatically.

Features

- Display memory
- Automatic signal generation
- Configurable frame frequency
- Blinking capability
- Regulated charge pump
- Contrast control by software
- Support for 4 types of LCDs:
  - Static
  - 2-mux, 1/2 bias or 1/3 bias
  - 3-mux, 1/2 bias or 1/3 bias
  - 4-mux, 1/2 bias or 1/3 bias

resulting contrast ratios between the on and off states.

Table 26–1.LCD Voltage and Biasing Characteristics

Mode	Bias Config	LCDMx	LCD2B	COM Lines	Voltage Levels	$V_{RMS,OFF}/V_{LCD}$	$V_{RMS,ON}/V_{LCD}$	Contrast Ratio $V_{RMS,ON}/V_{RMS,OFF}$
Static	Static	00	X	1	V1, V5	0	1	1/0
2-mux	1/2	01	1	2	V1, V3, V5	0.354	0.791	2.236
2-mux	1/3	01	0	2	V1, V2, V4, V5	0.333	0.745	2.236
3-mux	1/2	10	1	3	V1, V3, V5	0.408	0.707	1.732
3-mux	1/3	10	0	3	V1, V2, V4, V5	0.333	0.638	1.915
4-mux	1/2	11	1	4	V1, V3, V5	0.433	0.661	1.528

LCD_A (2/10)→ LCD Freq. Selection?

- The LCD_A controller uses the fLCD signal from the integrated ACLK prescaler to generate the timing for common and segment lines. ACLK is assumed to be 32768 Hz for generating fLCD.
- The proper fLCD frequency depends on the LCD's requirement for framing frequency and the LCD multiplex rate and is calculated by:
  - fLCD = 2 × mux × fFrame
- For example, to calculate fLCD for a 3-mux LCD, with a frame frequency of 30 Hz to 100 Hz:

fFrame (from LCD data sheet) = 30 Hz to 100 Hz

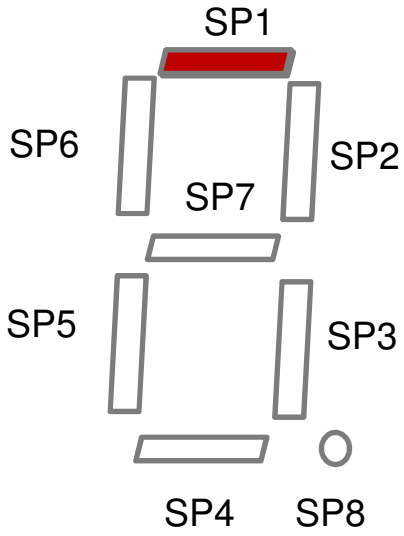
fLCD(min) = 180 Hz, fLCD(max) = 600 Hz

select fLCD = 32768/128 = 256 Hz or 2768/96 = 341 Hz or 32768/64 = 512 Hz.

- The lowest frequency has the lowest current consumption. The highest frequency has the least flicker.

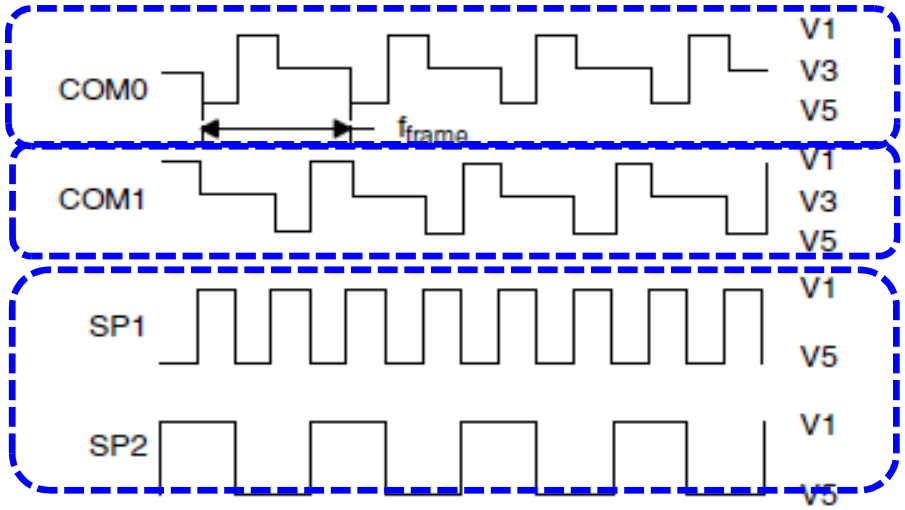
LCD_A (3/10) – Static Mode

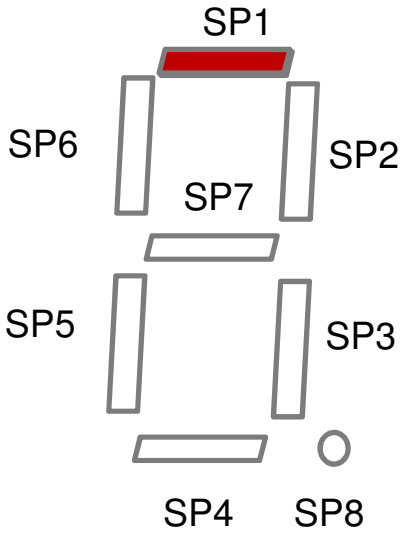
- In static mode, each MSP430 segment pin drives one LCD segment and one common line, COM0. SP → Segment Pin

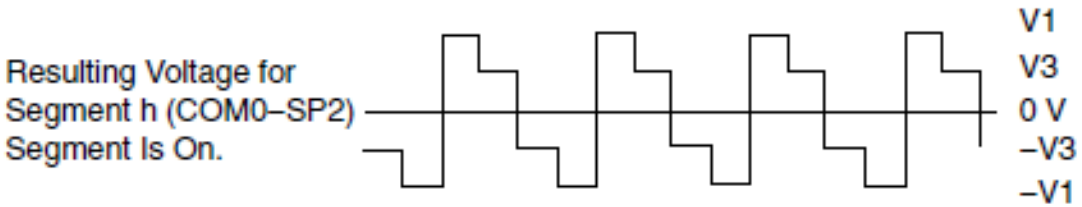


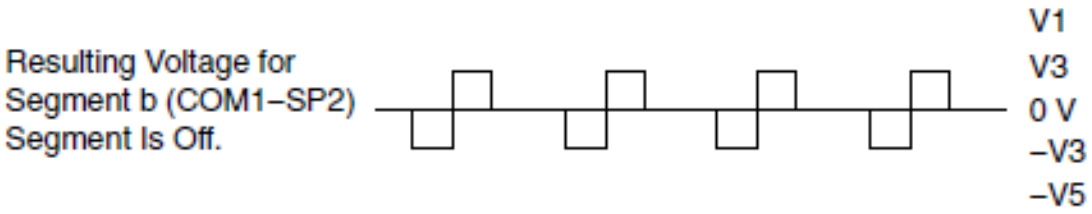
LCD_A (4/10) – 2 Mux Mode

- In 2-mux mode, each MSP430 segment pin drives two LCD segments and two common lines, COM0 and COM1, are used.



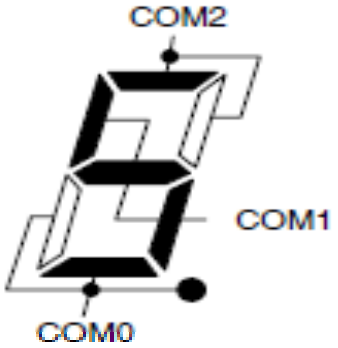




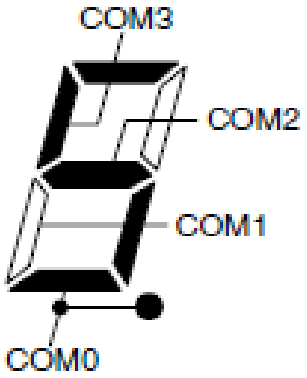


LCD_A (5/10) 3 Mux and 4 Mux Modes Waveforms not explained here.

- In 3-mux mode, each MSP430 segment pin drives three LCD segments and three common lines (COM0, COM1, and COM2) are used.



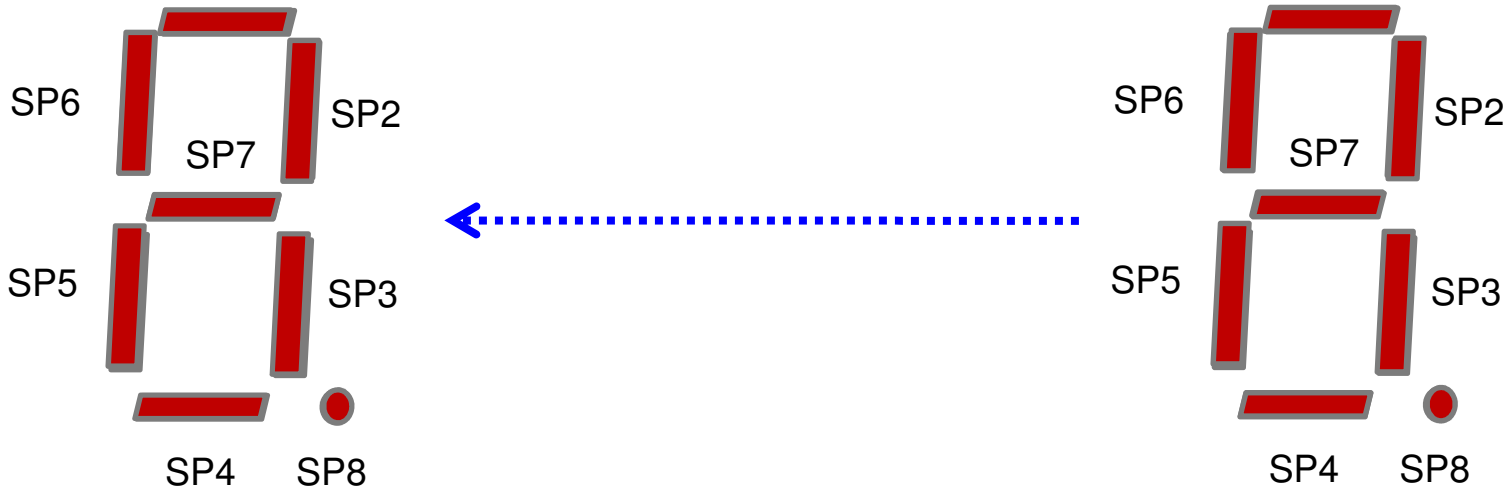
- In 4-mux mode, each MSP430 segment pin drives four LCD segments and all four common lines (COM0, COM1, COM2, and COM3) are used



LCD_A (6/10) - Static

With 30 segment lines, Max 4 digits can be supported

LCD_A (7/10) – 2 Mux



With 30 segment lines, Max 8 digits can be supported

LCD_A (8/10) – 3 Mux

DIGIT 10

DIGIT 1

With 30 segment lines, Max 10 digits can be supported

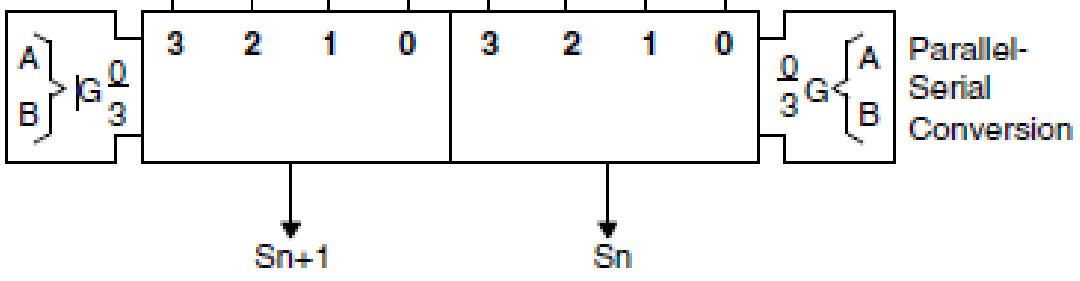
LCD_A (9/10) – 4 Mux

With 30 segment lines, Max 15 digits can be supported

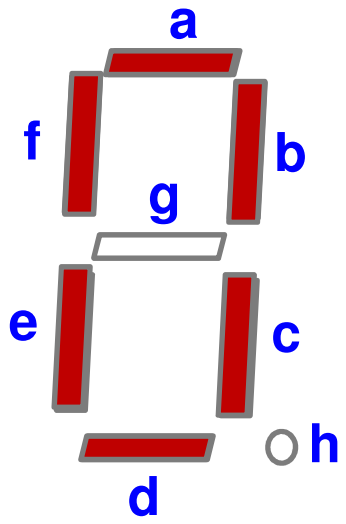
LCD_A (10/10) – Displaying

Display Memory

	COM	3	2	1	0	3	2	1	0		
MAB	09Fh	a	b	c	h	f	g	e	d	n = 30	Digit 16
	09Eh	a	b	c	h	f	g	e	d	28	Digit 15
	09Dh	a	b	c	h	f	g	e	d	26	Digit 14
	09Ch	a	b	c	h	f	g	e	d	24	Digit 13
	09Bh	a	b	c	h	f	g	e	d	22	Digit 12
	09Ah	a	b	c	h	f	g	e	d	20	Digit 11
	099h	a	b	c	h	f	g	e	d	18	Digit 10
	098h	a	b	c	h	f	g	e	d	16	Digit 9
	097h	a	b	c	h	f	g	e	d	14	Digit 8
	096h	a	b	c	h	f	g	e	d	12	Digit 7
	095h	a	b	c	h	f	g	e	d	10	Digit 6
	094h	a	b	c	h	f	g	e	d	8	Digit 5
	093h	a	b	c	h	f	g	e	d	6	Digit 4
	092h	a	b	c	h	f	g	e	d	4	Digit 3
	091h	a	b	c	h	f	g	e	d	2	Digit 2
										0	Digit 1



a+b+c+d+e+f = 0xEB



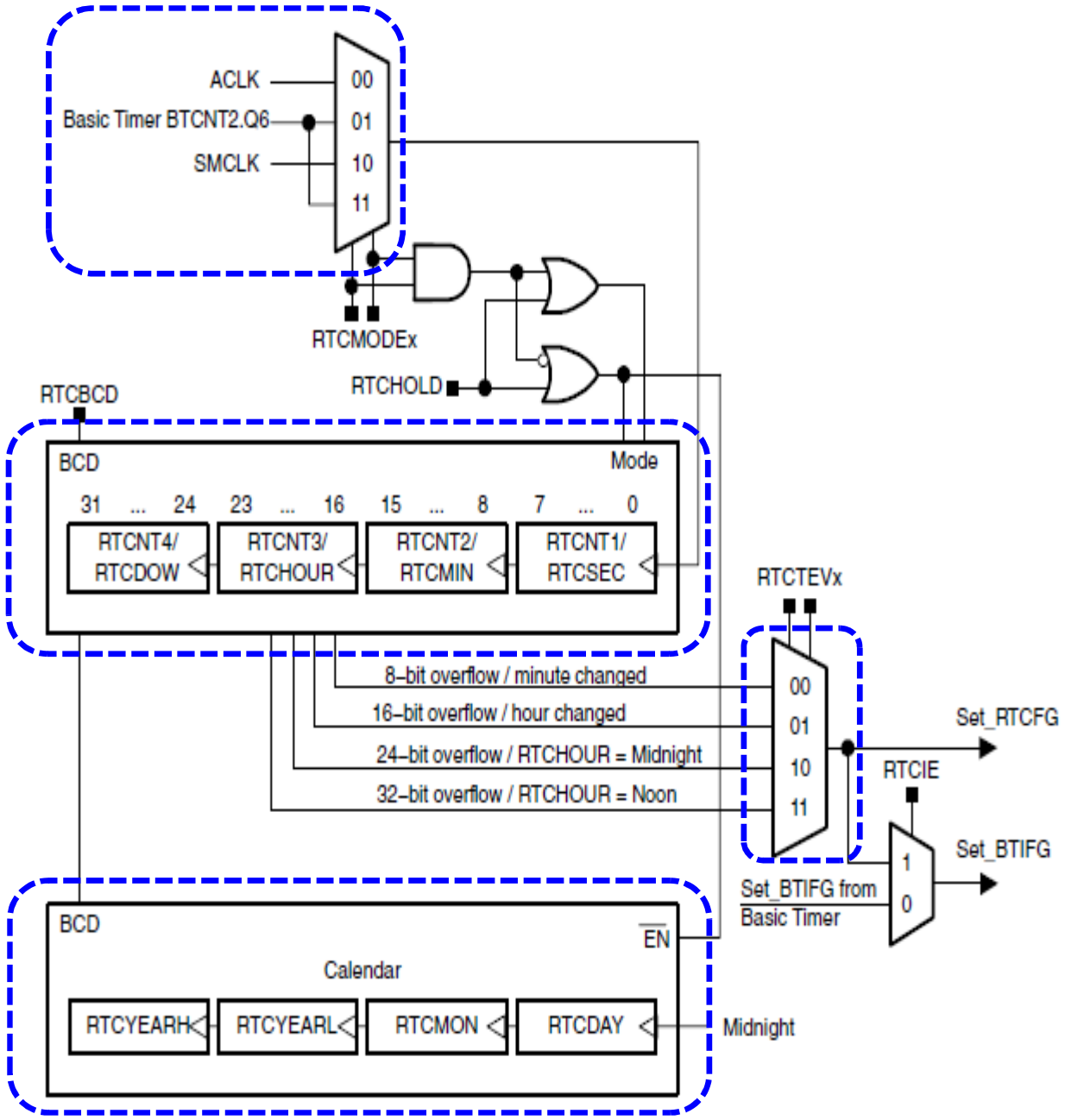
Each bit in the memory represents one segment or not used (mode based)

RTC (1/2)

- The Real-Time Clock (RTC) module can be used as a general-purpose 32-bit timer or as a RTC with calendar function.
- RTC features include:
  - Calendar and clock mode
  - 32-bit counter mode with selectable clock sources
  - Automatic counting of seconds, minutes, hours, day of week, day of month, month and year in calender mode.
  - Interrupt capability
  - Selectable BCD format

RTC (2/2)

- Clock source selection
- Counters
- Calendar
- Basic Timer Interaction
- Interrupt flags



Wrap-Up

- MSP430 peripherals – III
  - DMA
  - LCD

Q & A

Back-Up